Statement of Volatility – Dell PowerEdge C6320

The Dell PowerEdge C6320 contain both volatile and non-volatile (NV) components. Volatile components lose their data immediately upon removal of power from the component. Non-volatile components continue to retain their data even after the power has been removed from the component. Components chosen as user-definable configuration options (those not soldered to the motherboard) are not included in the Statement of Volatility. Configuration option information (pertinent to options such as microprocessors, remote access controllers, and storage controllers) is available by component separately. The following NV components are present in the PowerEdge C6320 servers.

Item	Non-Volatile or Volatile	Quantity	Reference Designator	
Planar				
PCH Internal CMOS RAM	Non-Volatile	1	U13	256 bytes
BIOS Password	Non-Volatile	1	U114	32 bytes
BIOS SPI Flash	Non-Volatile	1	U114	16M bytes
iDRAC SPI Flash	Non-Volatile	1	U126	4M bytes
BMC EMMC	Non-Volatile	1	U129	4G bytes
CPU Vcore Regulators	Non-Volatile	2	U99, U119	512 bytes
System CPLD RAM	Volatile	1	U143	1K bytes (8k bits)
System Memory	Volatile	Up to 8 per CPU	DIMM1 ~ DIMM16	Up to 32GB per DIMM
CPU	Volatile	1 or 2	CPU1 / CPU2	Various
iDRAC DDR	Volatile	1	U123	256M bytes
iDRAC	Volatile	1	U122	64K bytes + registers
LOM EEPROM	Non-Volatile	1	U66	64K bytes
LOM Flash	Non-Volatile	1	U61	1M bytes (8Mb)
24x2.5" MCU/Backplane				
MCU	Non-Volatile	5	U1,U2,U3,U4,U5	24K bytes Flash+ 8k bytes SRAM
Expander BP (RTS+)				
SPI Flash	Non-Volatile	1	U2	4M bytes
12x3.5" MCU Backplane				
MCU	Non-Volatile	5	U1,U2,U3,U4,U5	24K bytes Flash+ 8k bytes SRAM
FCB				
H8	Non-Volatile	1	U12	384K bytes(ROM)+40K Bytes (RAM)
CPLD	Non-Volatile	1	U15	64K bytes EBR SRAM
FRU	Non-Volatile	1	U18	32k bytes
Mid-plane				
EEPROM	Non-Volatile	2	U2,U15	4k bytes
H730 ,PERC (RTS+)				
NVSRAM	Non-volatile	1	U1033	128KB
FRU	Non-volatile	1	U1019	256B
1-Wire EEPROM	Non-volatile	1	U1004	128B
SPD	Non-volatile	1	U22	256B
SBR	Non-volatile	1	U1020	8KB
Flash	Non-volatile	1	U1031	16MB
ONFI Backup Flash	Non-volatile	1	U1059	4GB
SDRAM	Volatile	5	U1043-U1047	512MB/1GB
H330, PERC				
NVSRAM	Non-volatile	1	U1033	128KB
FRU	Non-volatile	1	U1019	256B
1-Wire EEPROM	Non-volatile	1	U1004	128B

Item	Non-Volatile or Volatile	Quantity	Reference Designator	
SBR	Non-volatile	1	U1020	8KB
Flash	Non-volatile	1	U3	16MB
LSI2008				
EEPROM	Non-volatile	1	U5	8k bytes
FLASH	Non-volatile	1	U4	16M bytes
1G NIC MEZZ				
SPI Flash	Non-volatile	1	U4000	1M bytes
EEPROM	Non-volatile	1	U11	32K bytes
10G NIC MEZZ				
SPI Flash	Non-volatile	1	U4000	2M bytes

Item	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)
Planar			
PCH Internal CMOS RAM	Battery-backed CMOS RAM	No	Real-time clock and BIOS configuration settings
BIOS Password	Battery-backed CMOS RAM	Yes	Password to change BIOS settings
BIOS SPI Flash	SPI Flash	No	Boot code, system configuration information, UEFI environment, Flash descriptor, ME
iDRAC SPI Flash	SPI Flash	No	iDRAC Uboot (bootloader), server management persistent store (i.e. IDRAC MAC Address, iDRAC boot variables), lifecycle log cache, virtual planar FRU and EPPID, rac log, system event log, JobStore, iDRAC Secure boot code,
BMC EMMC	eMMC NAND Flash	No	Operational iDRAC FW, Lifecycle Controller (LC) USC partition, LC service diags, LC OS drivers, USC firmware
CPU Vcore Regulators	ROM	No	Operational parameters
System CPLD RAM	RAM	No	Not utilized
System Memory	DRAM	Yes	System OS RAM
CPU	Cache + registers	Yes	Processor cache + registers
iDRAC DDR	DRAM	No	iDRAC local memory

Item	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)
iDRAC	Cache + registers	No	Processor cache + registers
LOM EEPROM	EEPROM	No	Onboard LOM FW
LOM Flash	Flash	No	Onboard LOM FW
24x2.5" MCU/Backplane			
MCU	Flash+SRAM	No	To decode LED blinking pattern
Expander BP (RTS+)			
SPI Flash	Flash	No	Expander firmware
12x3.5" MCU Backplane			
MCU	Flash+SRAM	No	To decode LED blinking pattern
FCB			
H8	ROM+RAM	No	FCB firmware
CPLD	EBR SRAM	No	Predominately for power sequence, watchdog and FAN control.
FRU	FRU	No	FAN table
Mid-plane			
EEPROM	EEPROM	No	SAS/SATA re-driver settings.
H730, PERC (RTS+)			
NVSRAM	NVSRAM	No	Configuration data
FRU	FRU	No	Card manufacturing information
1-Wire EEPROM	1-Wire EEPROM	No	Holds default controller properties/settings
SPD	SPD	No	Memory configuration data
SBR	SBR	No	Bootloader
Flash	Flash	No	Card firmware
ONFI Backup Flash	ONFI Backup Flash	No	Holds cache data during power loss
SDRAM	SDRAM	No	Cache for HDD I/O
H330, PERC			
NVSRAM	NVSRAM	No	Configuration data
FRU	FRU	No	Card manufacturing information
1-Wire EEPROM	1-Wire EEPROM	No	Holds default controller properties/settings
SBR	SBR	No	Bootloader
Flash	Flash	No	Card firmware
LSI2008			
EEPROM	EEPROM	No	Card Configuration
FLASH	FLASH	No	Card firmware

Item	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)
1G NIC MEZZ			
SPI Flash	Flash	No	Card firmware
EEPROM	EEPROM	No	Card firmware
10G NIC MEZZ			
SPI Flash	Flash	No	Card firmware

Item	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
Planar			
PCH Internal CMOS RAM	BIOS	N/A – BIOS only control	1) Set NVRAM_CLR jumper to clear BIOS configuration settings at boot and reboot system; 2) AC power off system, remove coin cell battery for 30 seconds, replace battery and power back on; 3) restore default configuration in F2 system setup menu.
BIOS Password	Keyboard	N/A	Place shunt on J_PSWD_NVRAM jumper pins 2 and 4.
BIOS SPI Flash	SPI interface via iDRAC	Software write protected	Not possible with any utilities or applications and system is not functional if corrupted/removed.
iDRAC SPI Flash	SPI interface via iDRAC	Embedded iDRAC subsystem firmware actively controls sub area based write protection as needed.	Not completely user clearable; however, user data, lifecycle log and archive, SEL, fw image repository can be cleared via Delete Configuration and Retire System, accessible in Lifecycle Controller interface
BMC EMMC	NAND Flash interface via iDRAC	Embedded FW write protected	Not completely user clearable; however, user data, lifecycle log and archive, SEL, fw image repository can be cleared via Delete Configuration and Retire System, accessible in Lifecycle Controller interface
CPU Vcore Regulators	Used Vender dongle and through software.	NA	Not user clearable
System CPLD RAM	Not utilized	Not accessible	Not accessible
System Memory	System OS	OS Control	Reboot or power down system
CPU	Various	Various	Power off
iDRAC DDR	iDRAC Firmware	NA	Power off
iDRAC	iDRAC Firmware	NA	Power off
LOM EEPROM	SPI interface via i350	NA	Not user clearable

Item	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
LOM Flash	SPI interface via i350	NA	Not user clearable
24x2.5" MCU/Backplane			
MCU	Pre-programmed before assembly	Not WP	Not user clearable
Expander BP (RTS+)			
SPI Flash	Pre-programmed before assembly, can be updated via LSI adapter and LSI utility	Not WP	Not user clearable
12x3.5" MCU Backplane			
MCU	Pre-programmed before assembly	Not WP	Not user clearable
FCB			
H8	Pre-programmed before assembly, can be updated via DELL utility	Not WP	Not user clearable
CPLD	Pre-programmed before assembly	Not WP	Not user clearable
FRU	Pre-programmed before assembly	Not WP	Not user clearable
Mid-Plane			
EEPROM	Pre-programmed before assembly	Not WP	Not user clearable
H730, PERC (RTS+)			
NVSRAM	ROC writes configuration data to NVSRAM	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
FRU	Programmed at ICT during production.	Not WP	Cannot be cleared with existing tools available to the customer
1-Wire EEPROM	ROC writes data to this memory	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
SPD	Pre-programmed before assembly	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
SBR	Pre-programmed before assembly	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
Flash	Pre-programmed before assembly. Can be updated using Dell/LSI tools	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
ONFI Backup Flash	FPGA backs up DDR data to this device in case of a power failure	Not WP. Not visible to Host Processor	Flash can be cleared by powering up the card and allowing the controller to flush the contents to VDs. If the VDs are no longer available, cache can be cleared by going into controller bios and selecting Discard Preserved Cache.
SDRAM	ROC writes to this memory - using it as cache for data IO to HDDs	Not WP. Not visible to Host Processor	Cache can be cleared by powering off the card

Item	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
H330, PERC			
NVSRAM	ROC writes configuration data to NVSRAM	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
FRU	Programmed at ICT during production	Not WP	Cannot be cleared with existing tools available to the customer
1-Wire EEPROM	ROC writes data to this memory	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
SBR	Pre-programmed before assembly	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
Flash	Pre-programmed before assembly. Can be updated using Dell/LSI tools	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
LSI2008			
EEPROM	IOC writes configuration data to EEPROM	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
FLASH	Pre-programmed before assembly, can be updated via LSI utility	Not WP	Not user clearable
1G NIC MEZZ			
SPI Flash	Pre-programmed before assembly, can be updated via Intel/DELL utility	Not WP	Not user clearable
EEPROM	Pre-programmed before assembly, can be updated via Intel/DELL utility	Not WP	Not user clearable
10G NIC MEZZ			
SPI Flash	Pre-programmed before assembly, can be updated via Intel/DELL utility	Not WP	Not user clearable

For any information that you may need, direct your questions to your Dell Marketing contact.